We claim:

1. An integrated electrical circuit, comprising:

a plurality of structure planes including at least one element structure plane;

electrically active elements disposed on said at least one element structure plane;

at least one insulation layer disposed above said at least one element structure plane;

electrical connecting leads disposed at least one of within and above said insulation layer, at least a portion of said electrical connecting leads contain copper;

connection pieces disposed underneath said electrical connecting leads; and

at least one diffusion blocker disposed underneath said electrical connecting leads, said diffusion blocker at least one of impedes and prevents a diffusion of copper, said diffusion blocker configured as a blocker layer interrupted only in at least one of a region having contact holes formed therein and a region of said connection pieces, said blocker

layer disposed between said at least one element structure plane and said insulation layer.

2. The integrated electrical circuit according to claim 1, including a diffusion barrier for impeding a diffusion of copper disposed at at least one of a surface of said contact holes and said connection pieces.

3. The integrated electrical circuit according to claim 1, wherein said electrical connecting leads have a copper content that is at least 10 percent by weight.

4. The integrated electrical circuit according to claim 1, wherein said insulation layer contains at least one substance selected from the group consisting of semiconductor oxides, semiconductor nitrides, fluorinated semiconductor oxides, fluorinated (amorphous) carbon, nitrides including boron nitride, polymers and polymer compounds including polyimides, polystyrenes, polyethylenes, polycarbonates, polybenzoxazole (PBO), benzocyclobutene (BCB), parylene, and fluoropolymers.

5. The integrated electrical circuit according to claim 1, wherein said blocker layer contains one of nitrogen, oxygen, fluorine, and a compound thereof.

6. The integrated electrical circuit according to claim 5, wherein said blocker layer contains a nitride.

7. The integrated electrical circuit according to claim 6, wherein said blocker layer contains one of silicon nitride Si_3N_4 and tungsten silicon nitride WSi_xN.

8. The integrated electrical circuit according to claim 5, wherein said blocker layer contains an oxidized nitride.

9. The integrated electrical circuit according to claim 8, wherein said blocker layer contains at least one compound selected from the group consisting of silicon oxynitride SiON, silicon boron oxynitride SiBON, titanium oxynitride TiN_xO_y, tantalum oxynitride TaN_xO_y, and tungsten oxynitride WN_xO_y.

10. The integrated electrical circuit according to claim 5, wherein said blocker layer contains a fluorinated nitride.

11. The integrated electrical circuit as claimed in claim 10, wherein said blocker layer contains silicon fluorooxynitride SiOFN.

12. The integrated electrical circuit according to claim 5, wherein said blocker layer contains a metal oxide.

13. The integrated electrical circuit according to claim 5, wherein said blocker layer contains a material selected from the group consisting of titanium oxide TiO_2 and tantalum oxide Ta_2O_5.

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14. The integrated electrical circuit according to claim 1, wherein said blocker layer has a thickness of between 50 nm and 800 nm.

15. The integrated electrical circuit according to claim 1, wherein said blocker layer is one of a plurality of blocker layers.

16. The integrated electrical circuit according to claim 15, wherein said blocker layers are disposed on different ones of said structure planes.

17. The integrated electrical circuit according to claim 15, wherein an extent to which said blocker layers impede diffusion and prevent diffusion differs.

18. The integrated electrical circuit according to claim 1, including at least one further diffusion blocker bearing on at least a portion of said electrical connecting leads.

19. The integrated electrical circuit according to claim 18,

wherein said further diffusion blocker bears on at least one of side areas and lower edges of said portion of said electrical connecting leads.

20. The integrated electrical circuit according to claim 18, wherein said further diffusion blocker prevents bulk outdiffusion of copper into said insulation layer.

21. The integrated electrical circuit according to claim 18, wherein an extent to which said blocker layer impedes diffusion is greater than that of said further diffusion blocker.

22. The integrated electrical circuit according to claim 18, wherein said blocker layer has a thickness greater than that of said further diffusion blocker.

23. The integrated electrical circuit according to claim 18, wherein a diffusion through said blocker layer is less than 10% of a diffusion through said further diffusion blocker.

24. A method for fabricating an integrated electrical circuit, which comprises:

forming electrically active elements in a region of a surface of a semiconductor substrate;

applying at least one diffusion blocker as a continuous blocker layer on the electrically active elements;

subsequently, applying at least one insulation layer on the continuous blocker layer; and

forming copper-containing electrical connecting leads at least one of within and on the insulation layer.